IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1. (Currently Amended) A multiple-gate transistor comprising:

a channel region;

a logic gate adjacent a first side of said channel region;

a floating gate adjacent a second side of said channel region, wherein said first side is opposite said second side such that said channel region is between said first side and said second side; and

a programming gate adjacent said floating gate, wherein said floating gate is between said programming gate and said channel region,

wherein said logic gate performs a different function than said floating gate, wherein said logic gate performs a different function than said programming gate, and wherein said floating gate performs a different function than said programming gate.

2. (Original) The transistor in claim 1, further comprising a gate oxide between said channel region and said logic gate and a first insulator between said channel region and said floating gate, wherein said first insulator is thicker than said gate oxide.

3. (Original) The transistor in claim 1, wherein voltage in said logic gate causes said transistor to switch on and off.

4. (Original) The transistor in claim 1, wherein charge in said floating gate adjusts the threshold voltage of said transistor.

5. (Original) The transistor in claim 1, wherein said transistor comprises a fin-type field effect transistor (FinFET).

6. (Original) The transistor in claim 1, further comprising source and drain regions at ends of said channel region, wherein said channel region comprises the middle portion of a fin structure and said source and drain regions comprise end portions of said fin structure.

7. (Original) The transistor in claim 1, wherein said floating gate is electrically insulated from other structures.

8. (Currently Amended) A multiple-gate transistor comprising:

a channel region;

source and drain regions at ends of said channel region;

a gate oxide on a first side of said channel region;

a logic gate adjacent said first gate oxide, wherein said gate oxide is between said logic gate and said channel region;

a first insulator on a second side of said channel region, wherein said second side of said channel region is opposite said first side such that said channel region is between said first side and said second side;

a floating gate adjacent said first insulator, wherein said first insulator is between said floating gate and said channel region;

a second insulator adjacent said floating gate; and

a programming gate adjacent said second insulator, wherein said second insulator is between said programming gate and said floating gate,

wherein said logic gate performs a different function than said floating gate, wherein said logic gate performs a different function than said programming gate, and wherein said floating gate performs a different function than said programming gate.

9. (Original) The transistor in claim 8, wherein said first insulator is thicker than said gate oxide.

10. (Original) The transistor in claim 8, wherein voltage in said logic gate causes said transistor to switch on and off.

11. (Original) The transistor in claim 8, wherein charge in said floating gate adjusts the threshold voltage of said transistor.

12. (Original) The transistor in claim 8, wherein said transistor comprises a fin-type field effect transistor (FinFET).

13. (Original) The transistor in claim 8, wherein said channel region comprises the middle portion of a fin structure and said source and drain regions comprise end portions of said fin structure.

14. (Original) The transistor in claim 8, wherein said floating gate is electrically insulated from other structures.

15-28. (Canceled).

29. (Currently Amended) A multiple-gate transistor comprising:

a channel region;

a logic gate adjacent a first side of said channel region, wherein voltage in said logic gate causes said transistor to switch on and off;

a floating gate adjacent a second side of said channel region, wherein said first side is opposite said second side such that said channel region is between said first side and said second side, and wherein charge in said floating gate adjusts the threshold voltage of said transistor; and

a programming gate adjacent said floating gate, wherein said floating gate is between said programming gate and said channel region.

30. (Cancelled).

31. (Previously Presented) The transistor in claim 29, further comprising a gate oxide between said channel region and said logic gate and a first insulator between said channel region and said floating gate, wherein said first insulator is thicker than said gate oxide.

32. (Previously Presented) The transistor in claim 29, wherein said transistor comprises a fin-type field effect transistor (FinFET).

33. (Previously Presented) The transistor in claim 29, further comprising source and drain regions at ends of said channel region, wherein said channel region comprises the middle portion of a fin structure and said source and drain regions comprise end portions of said fin structure.

34. (Previously Presented) The transistor in claim 29, wherein said floating gate is electrically insulated from other structures.

35. (Currently Amended) A multiple-gate transistor comprising:

a channel region;

a logic gate adjacent a first side of said channel region, wherein voltage in said logic gate causes said transistor to switch on and off, and wherein said transistor comprises a fin-type field effect transistor (FinFET);

a floating gate adjacent a second side of said channel region, wherein said first side is opposite said second side such that said channel region is between said first side and said second side, and wherein charge in said floating gate adjusts the threshold voltage of said transistor; and

a programming gate adjacent said floating gate, wherein said floating gate is between said programming gate and said channel region.

36. (Currently Amended) The transistor in claim ~~34~~ 35, further comprising a gate oxide between said channel region and said logic gate and a first insulator between said channel region and said floating gate, wherein said first insulator is thicker than said gate oxide.

37. (Currently Amended) The transistor in claim ~~34~~ 35, further comprising source and drain regions at ends of said channel region, wherein said channel region comprises the middle portion of a fin structure and said source and drain regions comprise end portions of said fin structure.

38. (Currently Amended) The transistor in claim ~~34~~ 35, wherein said floating gate is electrically insulated from other structures.